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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/722,159	11/26/2003	Byung-Se So	SEC.1092	7038

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EXAMINER	
NGUYEN, DILINH P	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 01/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/722,159	SO, BYUNG-SE	
	Examiner	Art Unit	
	DiLinh Nguyen	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

This application contains claims 5-19 are drawn to an invention nonelected with traverse. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi et al. (U.S. Pub. 2003/0015733) (previously applied) in view of Perino et al. (U.S. Pat. 6621155) (previously applied).

Hayashi et al. disclose a multi-chip package, comprising:

a plurality of pins; and

a semiconductor chip includes,

an input/output pad PT2A-PT2C,

an input/output driver (Address Buffer Circuit 21, Command Decoder Circuit 25" or Word Driver Circuit 26) coupled to the input/output pad,

an internal circuit (30, 42 or 40),

and an internal pad (PD2A-PD2C) for coupling the input/output driver 21 and the internal circuit 42 (fig. 13).

Hayashi et al. do not explicitly disclose the input/output pad of the first semiconductor chip directly receives an input/output signal transmitted via a corresponding one of the pins of the multi-chip package, and wherein the second through Nth semiconductor chips indirectly receive the input/output signal via the internal pads, which are coupled to each other.

However, Perino et al. disclose a multi-chip package comprising:

internal pads of the first 920 through Nth semiconductor chips (910a-910d) are coupled to each other, wherein the input/output pad of the first semiconductor chip 920 directly receives an input/output signal transmitted via a corresponding one of the pins of the multi-chip package, and wherein the second through Nth semiconductor chips (910a-910d) indirectly receive the input/output signal via the internal pads, which are coupled to each other (fig. 9, column 14, lines 17 et seq.). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device structure of Hayashi et al. by having the internal pads of the chips are coupled to each other and the second through Nth semiconductor chips indirectly receive the input/output signal via the internal pads, as taught by Perino et al., in order to provide an IC device having stacked dies with effectively isolating pins to be on the multi-chip device (column 14, lines 29-30).

- Regarding claim 2, Perino et al. disclose that the internal pads are coupled to each other via a common pad installed at a substrate 130 (fig. 1).
- Regarding claim 3, Perino et al. disclose that the input/output pad of the first semiconductor chip 920 is bonded to one of the pins of the multi-chip package (fig. 9).

- Regarding claim 4, it would have been obvious to one having ordinary skill in the art to have each of the first through (N-1)th semiconductor chips includes a delay circuit for receiving the input/output signal simultaneously with the internal circuit of the Nth semiconductor chip in order to use the semiconductor chip package in a particular application. Note Morgan (2003/0234674) (fig. 10, IC Die 1002, Delay Circuits 300-700), and Ishikawa (2003/0028835) (fig. 11, Chip 100, Delay Circuits 42, 43 and 45) are cited to support for the well known position.

Response to Arguments

Applicant's arguments filed 11/7/05 have been fully considered but they are not persuasive.

- The applicant argues that Hayashi discloses the chips 1 and 2 are connected by the pads PD1 and PD2; however, the pads PD1 and PD2 do not correspond to the recited internal pads, at least because they do not coupling an input/output driver and an internal circuit.

Applicant's arguments have been considered but they are not persuasive because pads PD2A correspond to the recited internal pads, at least because they are coupling an input/output driver 21 and the internal circuit 42 (fig. 13) and the chips receive an input/output signal via the internal pads (PD2A-PD2C) (fig. 13).

- The applicant argues that Perino et al. do not disclose any internal pads recited in claim 1.

Applicant's argument has been considered but it is not persuasive because Perino et al. clearly disclose a lower chip 920 and a plurality of upper chips 910a-910d, wherein the chips comprise a plurality of internal pads on their surface (fig. 9).

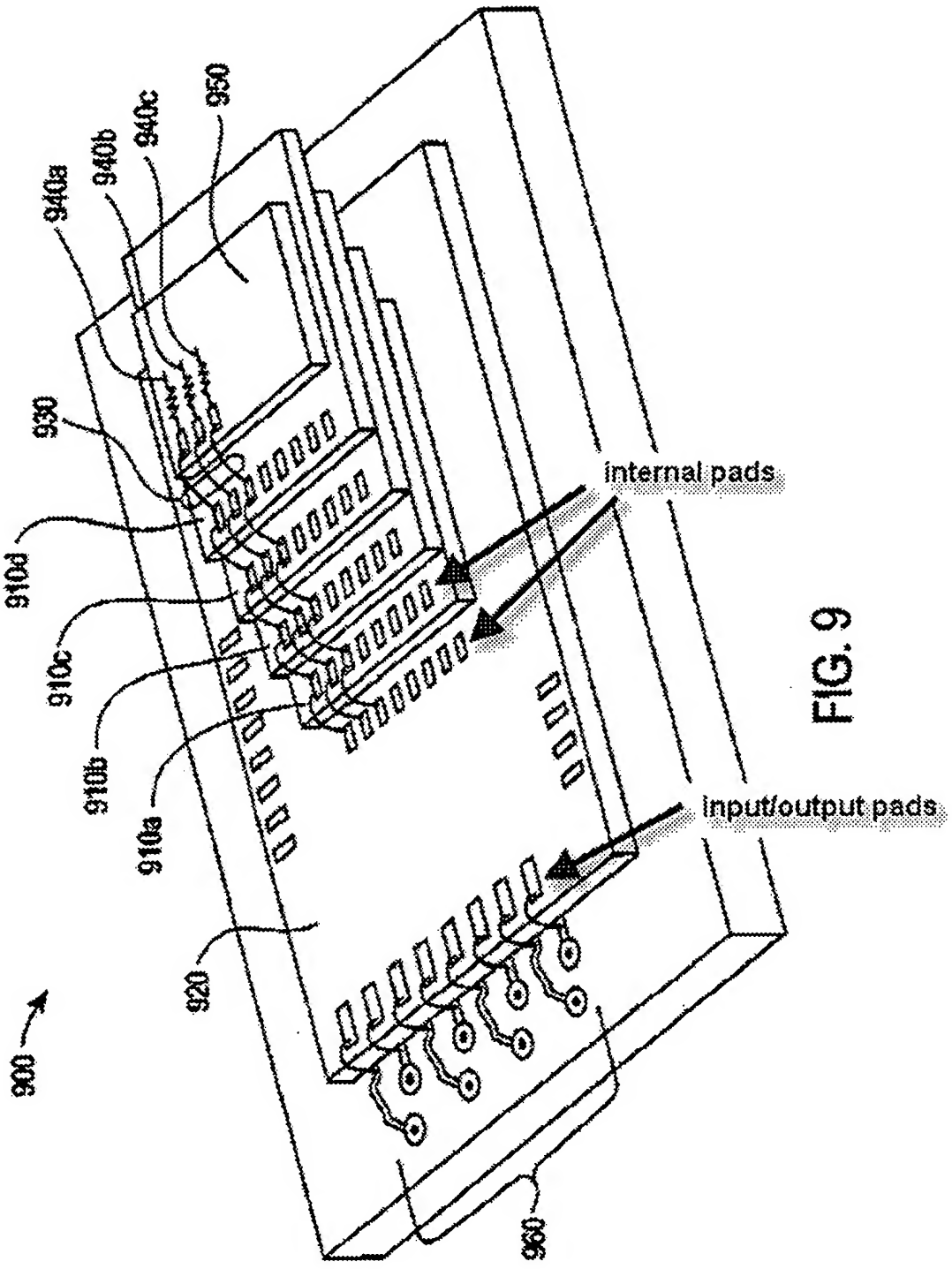
950
940c
940b
940a
930
910d
910c
910b
910a
920
900
internal pads
input/output pads
960

FIG. 9

- In response to applicant's argument that there is no motivation to combine the references, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

- In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case:

Hayashi et al. do not explicitly disclose the input/output pad of the first semiconductor chip directly receives an input/output signal transmitted via a corresponding one of the pins of the multi-chip package, and wherein the second through Nth semiconductor chips indirectly receive the input/output signal via the internal pads, which are coupled to each other.

However, Perino et al. disclose a multi-chip package comprising:

internal pads of the first 920 through Nth semiconductor chips (910a-910d) are coupled to each other, wherein the input/output pad of the first semiconductor chip 920

directly receives an input/output signal transmitted via a corresponding one of the pins of the multi-chip package, and wherein the second through Nth semiconductor chips (910a-910d) indirectly receive the input/output signal via the internal pads, which are coupled to each other (fig. 9, column 14, lines 17 et seq.). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device structure of Hayashi et al. by having the internal pads of the chips are coupled to each other and the second through Nth semiconductor chips indirectly receive the input/output signal via the internal pads, as taught by Perino et al., in order to provide an IC device having stacked dies with effectively isolating pins to be on the multi-chip device (column 14, lines 29-30).

- The applicant argues that Perino et al. do not disclose the internal pads are coupled to each other via a common pad installed at a substrate.

Applicant's argument has been considered but it is not persuasive because Perino et al. clearly disclose that the internal pads are coupled to each other via a common pad installed at a substrate 130 (fig. 1).

- The applicant argues that Perino et al. do not disclose the input/output pad of the first semiconductor chip is bonded to one of the pins of the multi-chip package.

Applicant's argument has been considered but it is not persuasive because Perino et al. clearly disclose that the input/output pad of the first semiconductor chip 920 is bonded to one of the pins of the multi-chip package (fig. 9).

- The applicant argues that neither Hayashi et al. nor Perino et al. disclose a delay

circuit for receiving the input/output signal simultaneously with the internal circuit of the Nth semiconductor chip.

Applicant's argument has been considered but it is not persuasive because it would have been obvious to one having ordinary skill in the art to have each of the first through (N-1)th semiconductor chips includes a delay circuit for receiving the input/output signal simultaneously with the internal circuit of the Nth semiconductor chip in order to use the multi-chip package in a particular application. Note Morgan (2003/0234674) (fig. 10, IC Die 1002, Delay Circuits 300-700), and Ishikawa (2003/0028835) (fig. 11, Chip 100, Delay Circuits 42, 43 and 45) are cited to support for the well known position.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DiLinh Nguyen whose telephone number is (571) 272-1712. The examiner can normally be reached on 8:00AM - 6:00PM (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DLN

HOAI PHAM
PRIMARY EXAMINER